

## The CCB Sanyo Proprietary Interface

### INTRODUCTION

A number of Wolfson devices have been selected to support the Sanyo proprietary CCB control interface. The devices supporting this interface are the WM8802 and WM8803, S/PDIF Audio Interface Transceiver and Receiver, and the WM8770/71, 8-channel codecs.

The write interface has similarities to the SPI 3-wire interface in that it uses three control lines and a total 16 control address and data bits, but differs in that it requires an additional 8 CCB address bits. It should also be noted that the CCB interface is LSB first and the SPI interface is MSB first. The WM8802 and WM8803 are also capable of read operations using two of the write control lines and a separate output line for read operations. The following note explains the operation and timing of a CCB interface.

### CCB OPERATION

CCB Interface mode allows multiple devices to be controlled off a common 3-wire bus. Each device on the 3-wire bus has a CCB Address comprising of the first 8 bits of the control word (B3-B0 and A3-A0). This CCB Address can either distinguish an individual device such as in the WM8770/71 case or identify a bank of registers within a device such as with the S/PDIF devices.

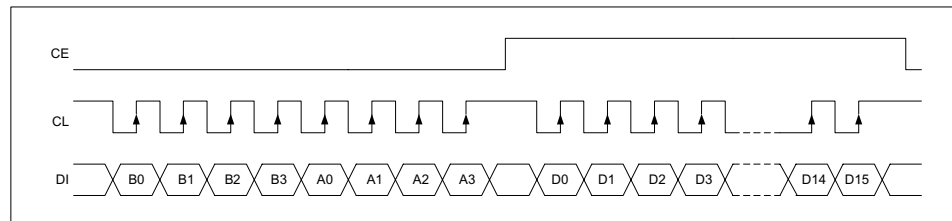
The WM8770 and WM8771 devices support write only CCB interface mode, whereas the S/PDIF devices support both read and write operation.

### WRITE OPERATION

The DI input is used for the CCB Address, register address and program data. CL is used to clock in the data on DI and is sampled on each of the rising edges of CL. CE low indicates the data on DI is the CCB Address; CE high indicates the program data for the WM8803 or the register address and program data for the WM8802 and WM8870/71.

The CCB Address is clocked in by eight CL clocks and is latched on the rising edge of CE. The sixteen CL clocks before a falling edge on CE will clock in the program data, or register address and program data; the data is latched on the falling edge of CE.

There is an advantage in maintaining the CL signal line in a high state when not writing to the device as this prevents false writes due to glitches; the clock sequence for this operation is shown in Figure 1.



**Figure 1 CCB Interface – Write Data CL Stopped High**

1. B[3:0] and A[3:0] are CCB Address bits. The WM8770/71 datasheet refers to these bits as A[7:0] and are the device address bits.
2. D[15:0] are Program bits or Address and Program bits.

It is possible to maintain the CL signal line in a low state when not writing to the device, the clock sequence for this operation is shown in Figure 2.

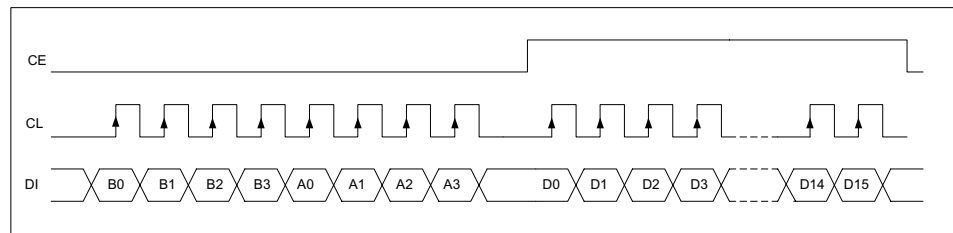


Figure 2 CCB Interface – Write Data CL Stopped Low

## READ OPERATION

During read operations the DI input is used solely for the CCB Address. CL is used to clock in the CCB Address bits and to clock out the read data on D0. DI and DO are sampled on the rising edges of CL. CE low indicates the data on DI is the read CCB Address; CE high indicates the read data is output on DO of the WM8802 or WM8803.

The CCB Address is clocked in on eight CL clocks and is latched on the rising edge of CE. The WM8802 device is capable of outputting up to 48 bits of read status data per register and the WM8803 up to 88 bits, dependent upon the register selected. This read data is latched on the falling edge of CE. Refer to the relevant device datasheet for details of the Read status register contents.

There is an advantage in maintaining the CL signal line in a high state when not writing to the device as this prevents false writes due to glitches; the clock sequence for this operation is shown in Figure 3.

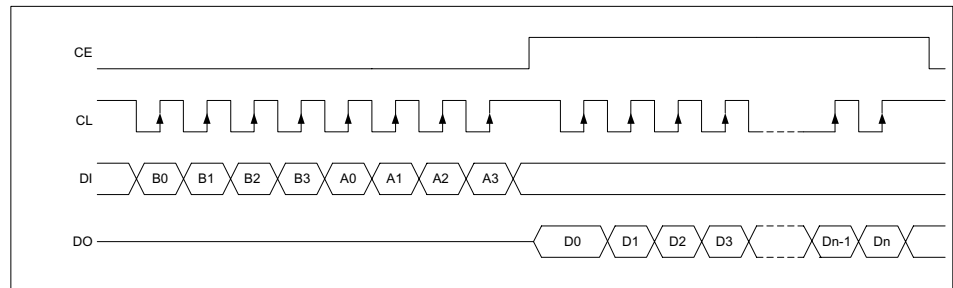


Figure 3 CCB Interface – Read Data CL Stopped High

1. B[3:0] and A[3:0] are CCB Address bits.
2. D[n:0] are Read status bits.

It is possible to maintain the CL line in a low state when not writing to the device, the clock sequence for this operation is shown in Figure 4.

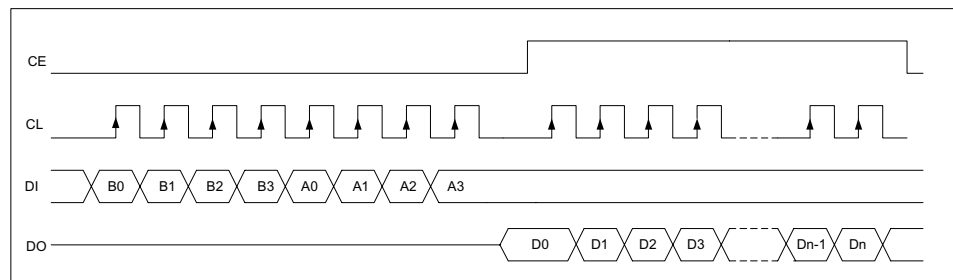


Figure 4 CCB Interface – Read Data CL Stopped Low

## BIT ALLOCATION SUMMARY

The three variations of control word bit allocation described above are summarized here.

### WM8770/71

In the WM8770/71 the device is addressed by the CCB Address and registers are selected by bits D15-D9.

A7 – A0	CCB Address bits
Write: D15 – D9	Register Address bits
	D8 – D0
	Program data bits
Read: n/a	

### WM8803

In the WM8803 the CCB Addresses are used to address single registers.

A7 – A0	CCB Address bits
Write: D15 – D0	Program data bits
Read: D87 – D0	Read status bits

### WM8802

In the WM8802 the CCB Address bits address a bank of registers within the device; each CCB Address has a number of its own registers that can also be accessed by Register bits D2-D7. Bits D0 and D1 are bits associated with a companion Sanyo micro-controller and are not required for use with other controllers.

A7 – A0	CCB Address
Write: D1 – D0	Associated Sanyo micro-controller address selection
	D7 – D2
	Register address within the selected CCB Address (A7 – A0)
	D15 – D8
	Program data bits
Read: D47 – D0	Read status bits

## SUMMARY

It is important to take into account the differences between the WM8770/71, WM8802 and WM8803 CCB words when implementing the control software for these devices. The Write commands use a constant 24 bits whereas the Read facilities can utilise between 48 and 88 bits of status data.

Control Interface hardware implementation is identical for the WM8802 and WM8803 but the WM8770 and WM8771 do not require a read line, as this facility is not available. It is of course possible to ignore the need for a read line when using the WM8802/03 S/PDIF devices if the status information is not required.

## APPLICATION SUPPORT

If you require more information or require technical support please contact Wolfson Microelectronics Applications group through the following channels:

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