

Minimising 'Pops' and 'Clicks' with the WM8759

INTRODUCTION

The WM8759 is an integrated DAC and headphone driver chip for applications such as portable MP3, CD or DVD. This note offers guidelines to help prevent 'pops' and 'clicks' when powering on or enabling the WM8759.

POP ON POWER-ON OF THE DEVICE

The WM8759 should always be powered on with the Enable pin held low. This holds the chip in its reset state and mutes the analogue outputs. A suitable power-on sequence would be:

1. Apply power (AVDD and DVDD)
2. Apply clocks and data (MCLK, LRCLK, BCLK, SDATA)
3. Switch Enable pin from Low to High

Note: The Enable pin must always be transitioned from Low to High after the power supplies have stabilised. If Enable is already high at power-on, the WM8759 can remain held in an unknown state (no output).

THUMP ON POWER-DOWN OF DEVICE

The WM8759 should ideally be powered-down with its Enable pin already held low. This will ensure that outputs are disabled before the device is shut down. A suitable power-down sequence would be:

1. Switch Enable pin from High to Low
2. Remove clocks and data (MCLK, LRCLK, BCLK, SDATA)
3. Remove power (AVDD and DVDD)

If Enable cannot be switched low before removing the supplies, a low level 'thump' will be heard on the outputs.

POP ON POWER-DOWN OF DEVICE (HIGH IMPEDANCE LOAD)

The WM8759 is designed primarily to drive headphone loads. If a line level load is to be driven then an additional low level load should be attached between the VOUTL/R and ground. A 300Ω load will allow significant reduction in power-down noise without affecting performance.

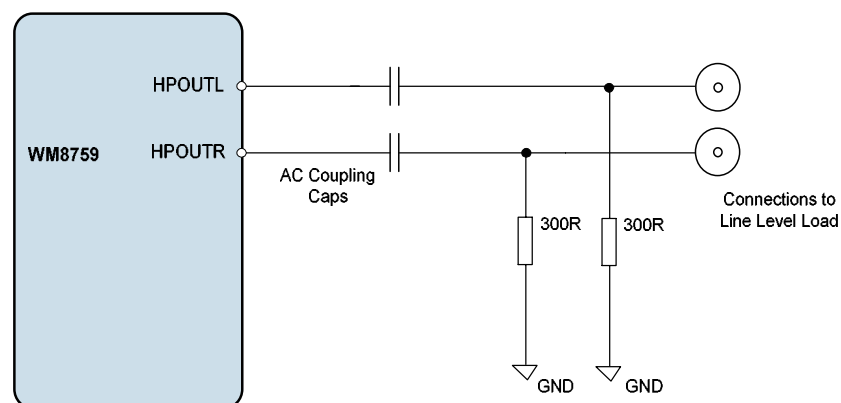


Figure 1 Low level Load in Parallel with Line Level Load

POP ON STARTING/STOPPING/ CLOCKS

Clock and data signals (MCLK, LRCLK, BCLK, SDATA) should not be applied or removed when the Enable pin is High. Applying and removing MCLK has the effect of powering up and down the DACs. If Enable is High, this will be heard as a pop on the outputs.

POP ON ENABLE

If a 'pop' is heard on Enable, it will be because the voltage on the VMID pin has not yet fully discharged. This is most evident when the device has been disabled and then enabled again after a very short period. On the WM8759 Evaluation board, the period for VMID to discharge to an acceptable level is around 30 seconds.

Factors that effect discharge time are the size of AC coupling capacitors on the outputs and the size of the decoupling capacitor on the VMID pin.

The WM8759 will Enable without any 'pop' at all once VMID has fallen to 20mV. In practice, a voltage of around 100mV will cause only a minimal 'pop'.

If it is important that the WM8759 should produce no 'pop' even when disabled/re-enabled in a very short period, a simple transistor circuit can be used to discharge VMID more quickly:

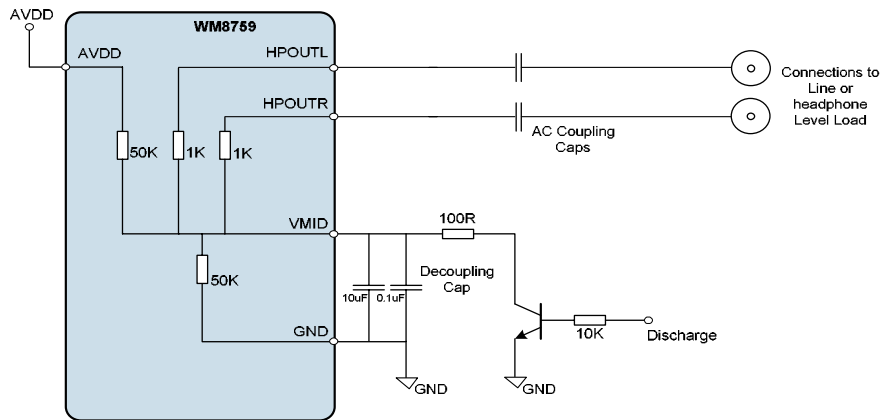


Figure 2 VMID and Discharge Circuit

The Discharge signal can be provided either by a free GPIO pin on a controller chip or simply by inverting the ENABLE signal so that VMID will be discharged immediately on Disable. An example of a circuit including such an inverter is shown in Figure 3.

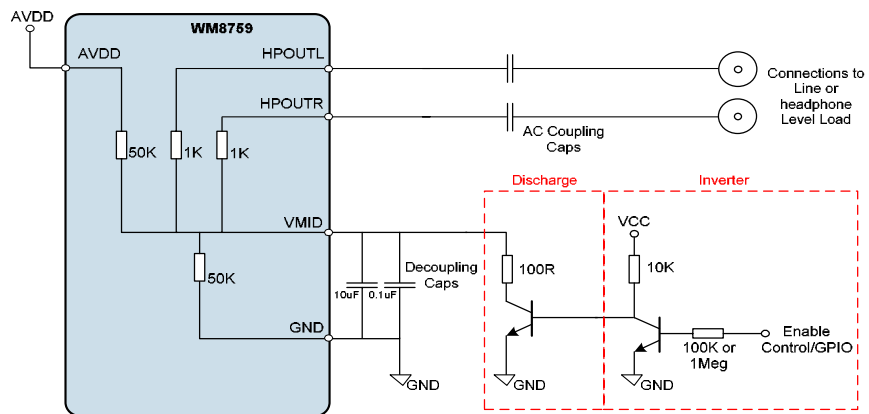


Figure 3 Discharge Circuit with Inverter

The circuit above can be used to discharge VMID using the existing Enable signal. This will automatically trigger the discharge circuit at the appropriate time.

APPLICATION SUPPORT

If you require more information or require technical support please contact Wolfson Microelectronics Applications group through the following channels:

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