



## DEVELOPMENT MODE

Although the predefined “custom modes” (3 per device) are designed to encompass several processors, there are solutions where these may not meet the exact requirements of the user’s application. In these instances the development mode can be used to set up the system exactly to the user’s requirements with just the addition of a few external components. Figure 2 shows a typical example of how the WM835x would be implemented in development mode.

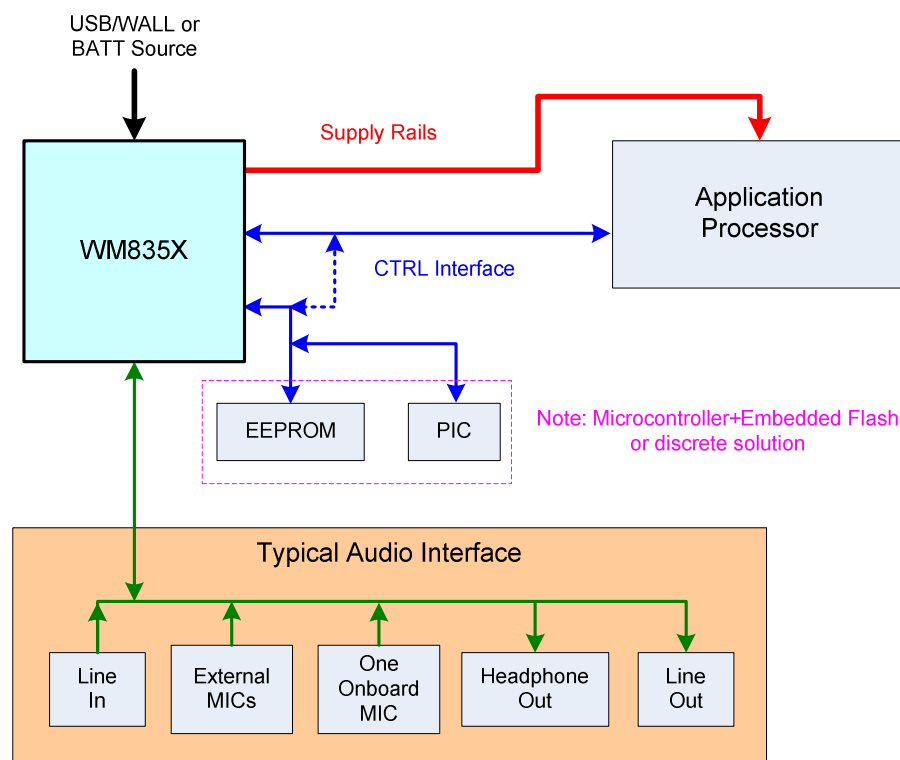


Figure 2 – WM835x System Diagram

## INITIALISING THE WM835x

In Development Mode, the WM835x must be initialised by writing to the relevant start-up registers. To allow this start-up sequence to be written and the required GPIO pins to be configured, an external source must be used. Typically this is a non-volatile EEPROM (note: the EEPROM could be the embedded Flash memory of a microcontroller) which will automatically download its contents to the WM835x when required.

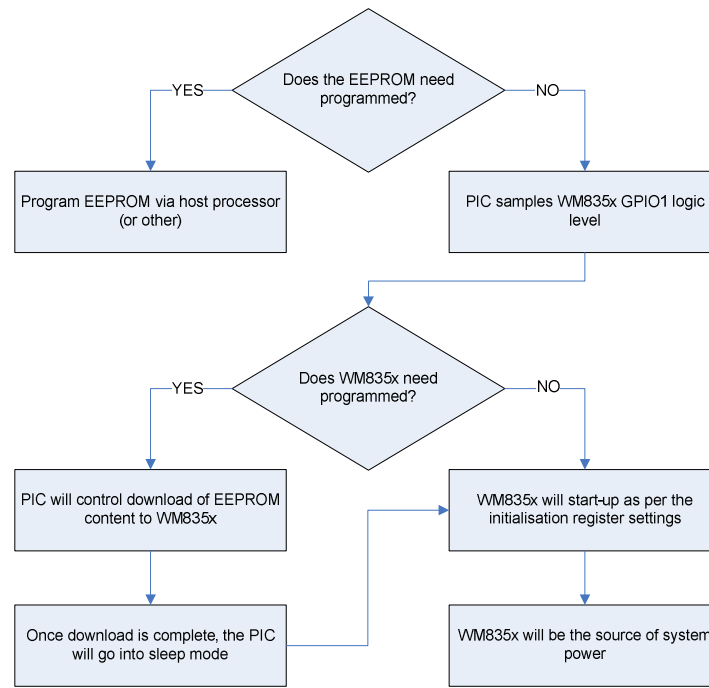
Operating the WM835x in Development Mode is achieved by setting the CONFIG pins (J1 (CONF0) & K1 (CONF1)) to 00 in hardware.

Once the start-up registers settings have been transmitted to the EEPROM, a full system power cycle will then allow the WM835x to power up and be programmed by the EEPROM.

A microcontroller (PIC) should be used to control the register writes from the EEPROM to the WM835x. GPIO1 of the WM835X can be used as a program flag (i.e. a DO\_CONF output). If the logic level of the pin at power-up is high, this signifies that the WM835x is programmed and the register settings have been held by the valid RTC supply. If the level on the GPIO1 pin is low, it highlights that the WM835x need to be programmed. The GPIO1 pin will be input to a GPIO on the PIC, after a POR the PIC will sample the logic level on the GPIO and if required, download the EEPROM content to the WM835x; otherwise if will go into sleep state waking only after a POR.

The control interface that is used to program the start-up sequence is on pins B11 (GPIO10) for SCLK and C10 (GPIO11) for SDATA; the secondary control interface which is enabled by defaults in standard mode.

Figure 3 shows the recommended initialisation through the start-up procedure.



**Figure 3 – WM835x Initialisation Procedure**

## CONTROL INTERFACE

The WM835x has the option to be controlled via the most widely used control interface i.e. I<sup>2</sup>C and SPI, as shown in Table 1 and Table 2.

Though, other control interfaces can be used, refer to WM835x datasheet section – “CONTROL INTERFACE” – for details.

<b>PRIMARY INTERFACE (SDATA &amp; SCLK) I<sup>2</sup>C address =</b> Selectable 0011010[R/W] (i.e. 0x34h); 0011011[R/W] (i.e. 0x36h); 0011110[R/W] (i.e. 0x3Ch); 0011111[R/W] (i.e. 0x3Eh) ( <i>The format is "Device ID + R/W bit"=8 bits in total.</i> )	
<b>SECONDARY INTERFACE (GPIO10 &amp; 11) I<sup>2</sup>C address =</b> 0011010[R/W] (i.e. 34) (default initialisation address)	
<b>I<sup>2</sup>C</b>	<b>WM835x</b>
SCL	SCLK (N2)
SDA	SDATA (M3)

Table 1 – I<sup>2</sup>C Interface

<b>SPI</b>	<b>WM835x</b>
SCLK	SCLK (N2)
CSB	GPIO7 (N4) (i.e. CSB)
SDIN	SDATA (M3)
SDOUT	GPIO6 (M4) (i.e. SDOUT)

Table 2 – SPI Interface

## SUGGESTED WM835X DEVELOPMENT MODE CONFIGURATION

Figure 4 shows a suggested WM835x configuration in Development Mode. A typical configuration sequence would include writes to some or all of the registers, which determine the WM8350x start-up behaviour.

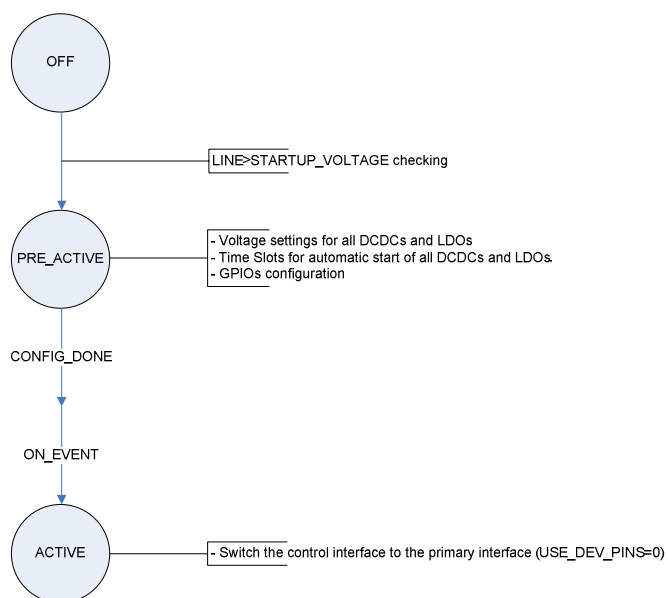


Figure 4 – WM835x Development Mode Configuration

Note that configuration only includes registers that are required for starting up correctly. All other registers should be loaded after the WM8350x has started up.

**RECOMMENDED GENIE CIRCUIT (PIC WITH EMBEDDED FLASH MEMORY)**

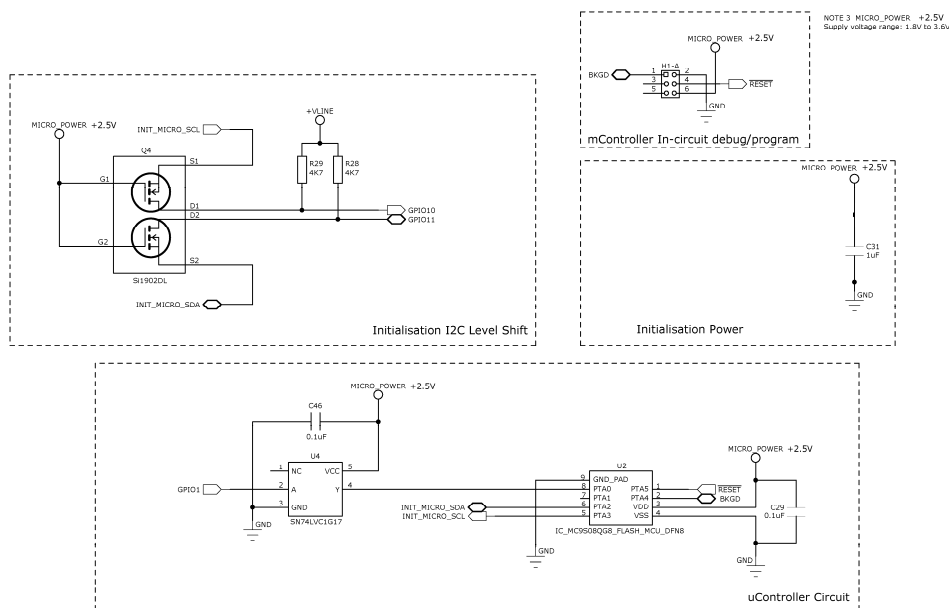
Wolfson recommend the use of a single chip microcontroller with an embedded Flash memory to configure the WM835x at start-up in Development Mode (see Table 3).

This provides a very cost effective solution due to the low-cost and small-size of the recommended microcontroller.

	<b>Recommended PIC</b>	<b>Alternative PIC</b>
<b>Part Number</b>	MC9S08QG8CFQE	PIC10F200/202/204/206
<b>Manufacture</b>	Freescale Semiconductor	Microchip
<b>Description</b>	Microcontroller, 8Bit MCU 8K Flash, 512Byte RAM, I <sup>2</sup> C/SPI	Microcontroller, 8Bit MCU 8K Flash, 256-512Byte RAM, CSP
<b>Package(s)</b>	DFN-8 (Dual Flat No lead-8pin SMD)	6-pin SOT23, 8-pin PDIP, DFN (Dual Flat No lead-8pin SMD)
<b>Cost</b>	\$ 0.81 (> 1000pcs)	< \$ 0.5 (>1000pcs)

**Table 3 – Recommended PIC (with embedded Flash memory)**

Figure 5 shows the recommended interface between the EEMPROM/PIC and the WM835x.



**Figure 5 – Recommended Genie Circuit**

The GPIO10 & GPIO11 pins are supported on the “LINE” power domain, therefore a level shift circuit is required if the control signals (i.e. SCL & SDA) are on different power domain.

The GPIO1 input is buffered using a single Schmitt-Trigger from TI (SN74LVC1G17DBVR).

An external regulated power supply set to 2.5V should be connected to “MICRO\_POWER +2.5V” (H1-A connector) to provide supply to the genie circuit. The range of the external regulated power supply should be 1.8V to 3.6V.

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**SUMMARY/CONCLUSION**

This application note has shown how the development mode of the WM835x family can be used where the predefined "custom modes" do not exactly fit the user requirements. This increases the number of application processors which can be powered by the WM835x and also allows increased flexibility for the user to change other elements of the system without the need to re-design power management solution, saving development time and cost. The WM835x power management is a versatile part providing high performance audio processing and power management which complement a range of application's processors.

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## **APPLICATION SUPPORT**

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