

Using the WM8753 for Bluetooth Record (PCM to I²S Conversion)

INTRODUCTION

The need to convert PCM to I²S data format is desirable in many multi-media phones with Bluetooth (BT) capability where the signal across the BT link is to be recorded.

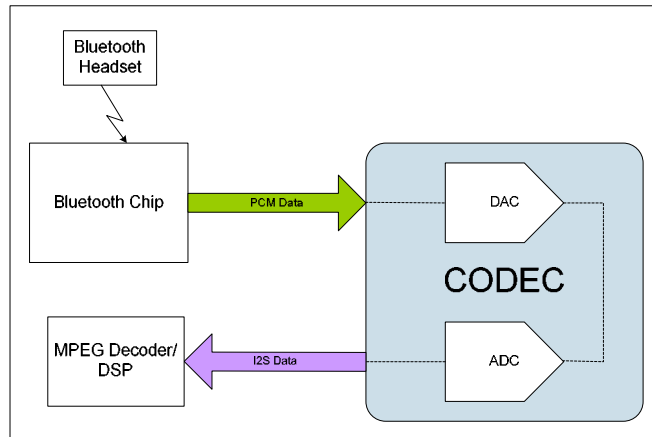


Figure 1 Typical Call Record Block Diagram

This conversion is required as the majority of BT IC's at present only output PCM formatted data while many DSP's will be setup to use I²S formatted data (Left Justified or Right Justified data may also be used).

The BT IC outputs PCM formatted data as it is ideal for voice signals. It is mono only and ideal for reduced sampling rates and bit rate due to only one channel being considered.

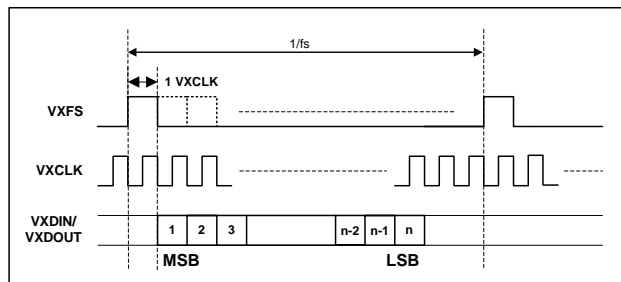


Figure 2 PCM Data Format Mode A

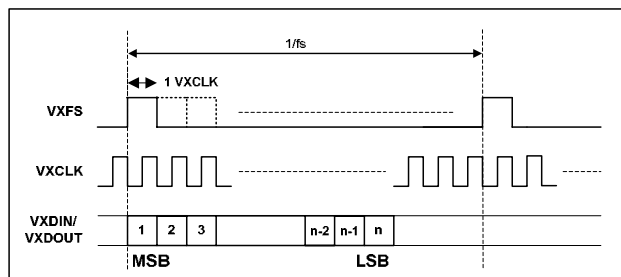


Figure 3 PCM Data Format Mode B

The DSP will typically use one of the standard audio data formats as it will be used to output stereo audio to headphones or on-phone speakers.

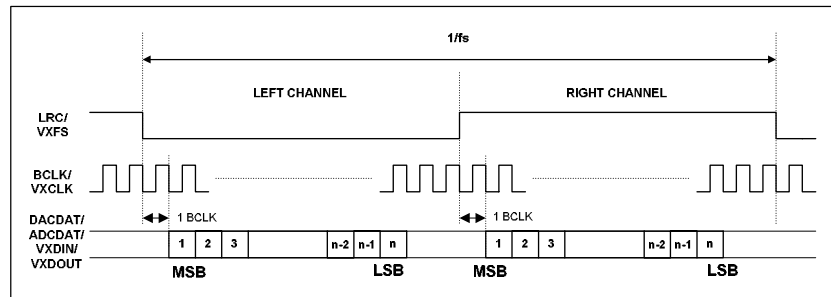


Figure 4 I²S Justified Data Format

The rising edge of VXFS alone signifies the start of a new frame in PCM format. The falling edge of VXFS is ignored. As can be seen in Figure 4, LRC low signifies left channel data while LRC high signifies right channel data.

There is no direct way to input PCM format data into an interface expecting I²S format data, a conversion must take place.

Due to the flexibility offered by the WM8753 this conversion can be done. There are some limitations however due to the WM8753 not being specifically designed to offer this conversion.

The aim of this application note is to provide a clear understanding of the WM8753 interfaces and their interaction. From this, it should become clear as to the possible solutions offered by the WM8753 and the considerations that must be made before design.

WM8753 AUDIO INTERFACE OPTIONS

The WM8753 has two very flexible audio interfaces. One interface has a connection to a mono voice DAC and a stereo ADC. The other interface has a connection to a stereo HiFi DAC. The flexibility offered by the WM8753 allows interconnection between the two interfaces as shown in Figure 5.

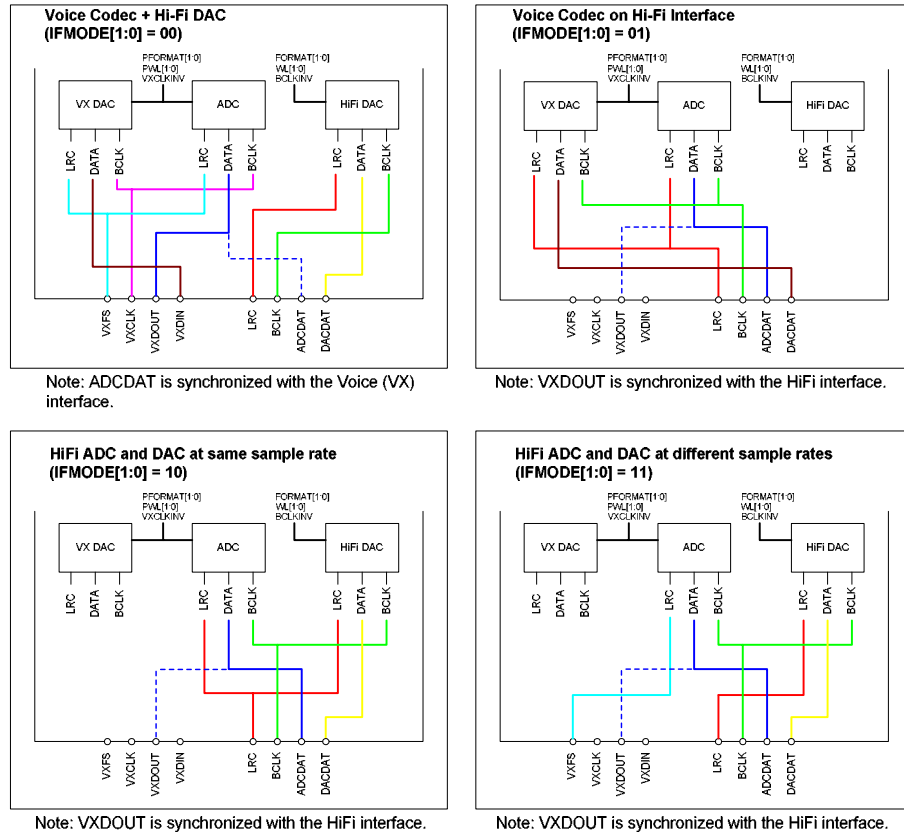


Figure 5 Audio Interface Routing Options

As can be seen, the Voice Interface (VXFS, VXCLK, VXDOU, VXDI) may be routed to the VX DAC and ADC only. The HiFi Interface (LRC, BCLK, ADCCAT, DACDAT) can be routed to the HiFi DAC, VX DAC and ADC. The different routing options are selected by setting the IFMODE register bits.

Both interfaces can be configured for any data format which is one of the advantages of the WM8753 making data conversion possible. The Voice Interface uses the PFORMAT and PWL register bits to set the data format and word length while the HiFi Interface uses the FORMAT and WL register bits. Refer to tables Table 1, Table 2 and Table 3.

WAN_0152

IFMODE[1:0]	DAC DATA	DAC FRAME SYNC	DAC BIT CLK	DAC WORDLENGTH	DAC FORMAT
00	DACDAT	LRC	BCLK	WL[1:0]	FORMAT[1:0]
01	DACDAT	LRC	BCLK	WL[1:0]	FORMAT[1:0]
10	DACDAT	LRC	BCLK	WL[1:0]	FORMAT[1:0]
11	DACDAT	LRC	BCLK	WL[1:0]	FORMAT[1:0]

Table 1 Hi-Fi DAC Audio Interface Configuration

IFMODE[1:0]	ADC DATA	ADC FRAME SYNC	ADC BIT CLK	ADC WORDLENGTH	ADC FORMAT
00	VXDOUT	VXFS	VXCLK	PWL[1:0]	PFORMAT[1:0]
01	ADCDAT	LRC	BCLK	PWL[1:0]	PFORMAT[1:0]
10	ADCDAT	LRC	BCLK	PWL[1:0]	PFORMAT[1:0]
11	ADCDAT	VXFS	BCLK	PWL[1:0]	PFORMAT[1:0]

Table 2 ADC Audio Interface Configuration

IFMODE[1:0]	VXDAC DATA	VXDAC FRAME SYNC	VXDAC BIT CLK	VXDAC WORDLENGTH	VXDAC FORMAT
00	VXDIN	VXFS	VXCLK	PWL[1:0]	PFORMAT[1:0]
01	DACDAT	LRC	BCLK	PWL[1:0]	PFORMAT[1:0]
10	-	-	-	-	-
11	-	-	-	-	-

Table 3 Voice DAC Audio Interface Configuration

See the latest WM8753 datasheet for more details.

To be able to convert PCM to I²S data format the following is needed:

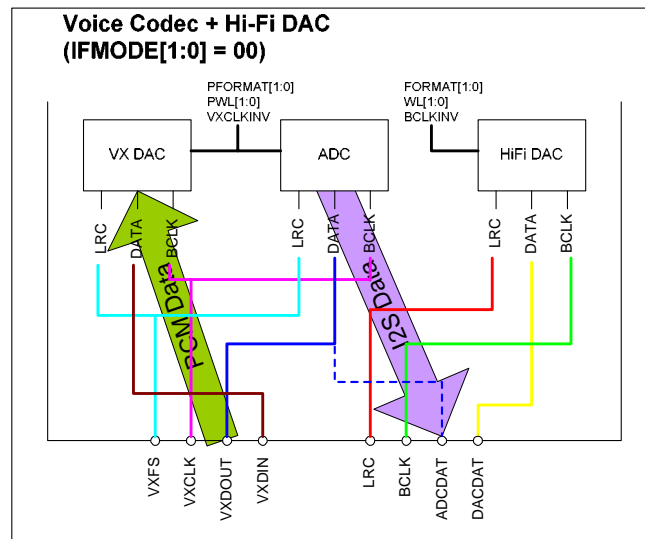
INTERFACE 1 (PCM INPUT)	INTERFACE 2 (I ² S OUTPUT)
PCM Frame Clock	I ² S Frame Clock
PCM Data Clock	I ² S Data Clock
PCM Digital Data Input	I ² S Digital Data Output

Table 4 Interface Signal Requirements

Figure 5 shows that IFMODE[1:0]=00 offers the best routing option to achieve a successful data conversion based on the signal requirements shown in Table 4.

IFMODE[1:0]=00 OPTIONS

PCM data input to Voice Interface – I²S data output from HiFi Interface



Note: ADCDAT is synchronized with the Voice (VX) interface.

Figure 6 IFMODE[1:0] = 00 Unsynchronized Output Example

The diagram shown in Figure 6 makes it immediately obvious that this combination of direct interface usage will not work. The main reason for this is stated in the note under the diagram; “ADCDAT is synchronized with the Voice (VX) interface”. The ADC data output is not synchronized to the HiFi interface meaning that the data will not be justified correctly for the I²S data output.

Whether the WM8753 is in Master mode (i.e. clocks are output) or Slave mode (i.e. clocks are input), the ADCDAT (I²S data output) is synchronised to the PCM timing rather than the required I²S timing.

Figure 7 is a scope capture of the setup timing described. The Voice and HiFi interfaces are in Master mode. The internal routing path is shown in Figure 11. As can be seen, the PCM data format (Mode A) is correct. The I²S frame clock (LRC) is correct but, the data is not sitting correctly within the frame.

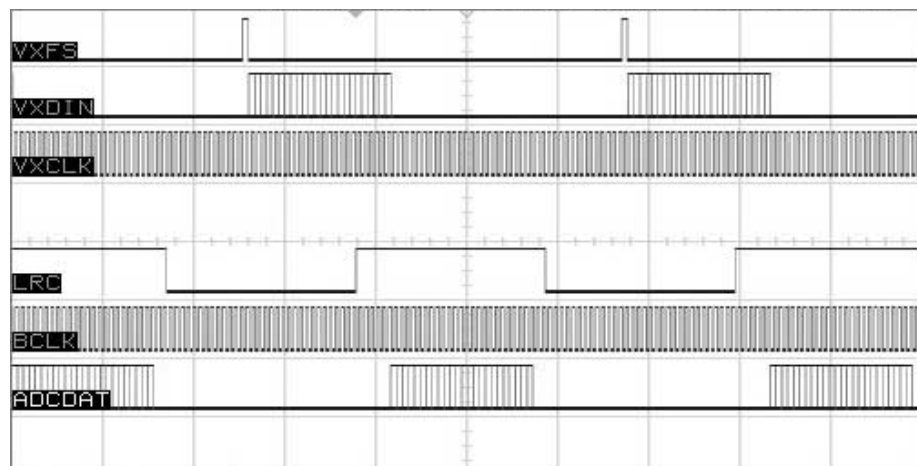


Figure 7 Out of Sync I²S Output Data Format

The solution to this synchronization issue requires the use of an external switch circuit. An example setup is shown in Figure 8.

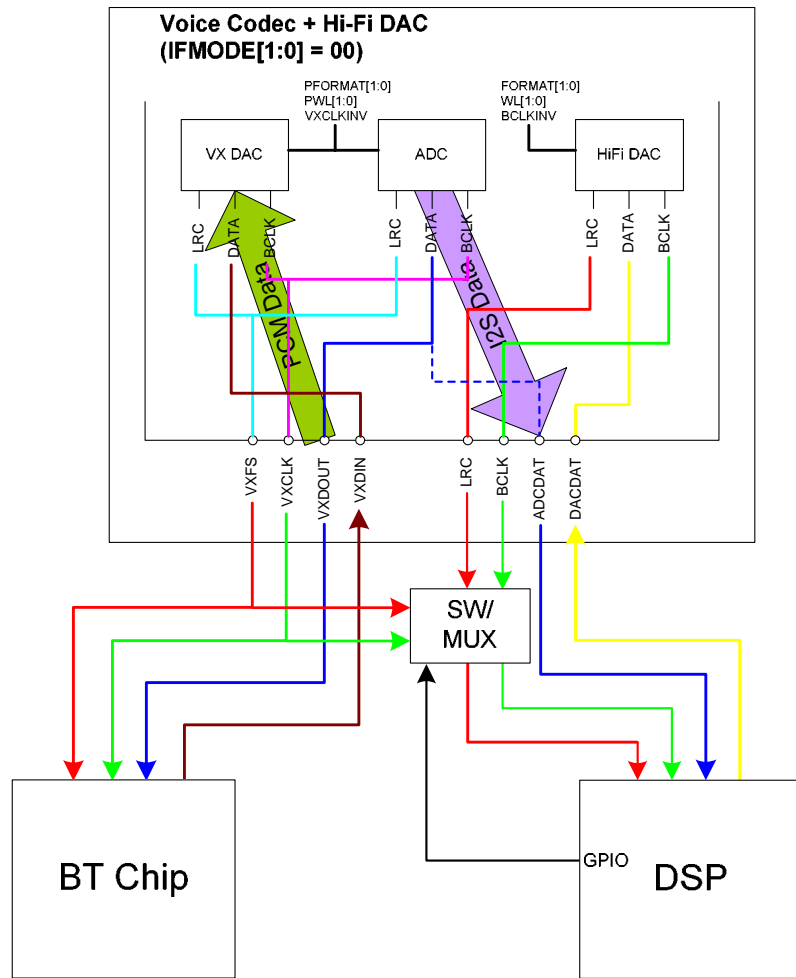


Figure 8 Possible Solution 1

The diagram in Figure 8 allows the VXDAC and ADC to be used purely for phone call purposes while the HiFi DAC may be used for audio playback of an MP3 file for example. This solution also allows the PCM to I²S conversion to take place.

One limitation of this solution is that a single frame sync is used meaning that both the PCM and I²S data must be running at the same sample rate. This also means that the frame sync edges must be the same for both PCM and I²S data. As stated previously, in PCM mode of the WM8753, it is the rising edge only that signifies the start of a new frame, the falling edge is ignored. This is also true for the many BT chips. Due to this, it is possible to apply an I²S frame sync signal to both the BT chip and the DSP via the sw/mux. In this case the ADCDAT is synchronized with the correct LRC and BITCLK. The BT chip will output data on the rising edge of VXFS (right channel data in I²S format).

If monitored on a scope, both interfaces will appear to have I²S timing and data format.

In this mode, the WM8753 must be the Master.

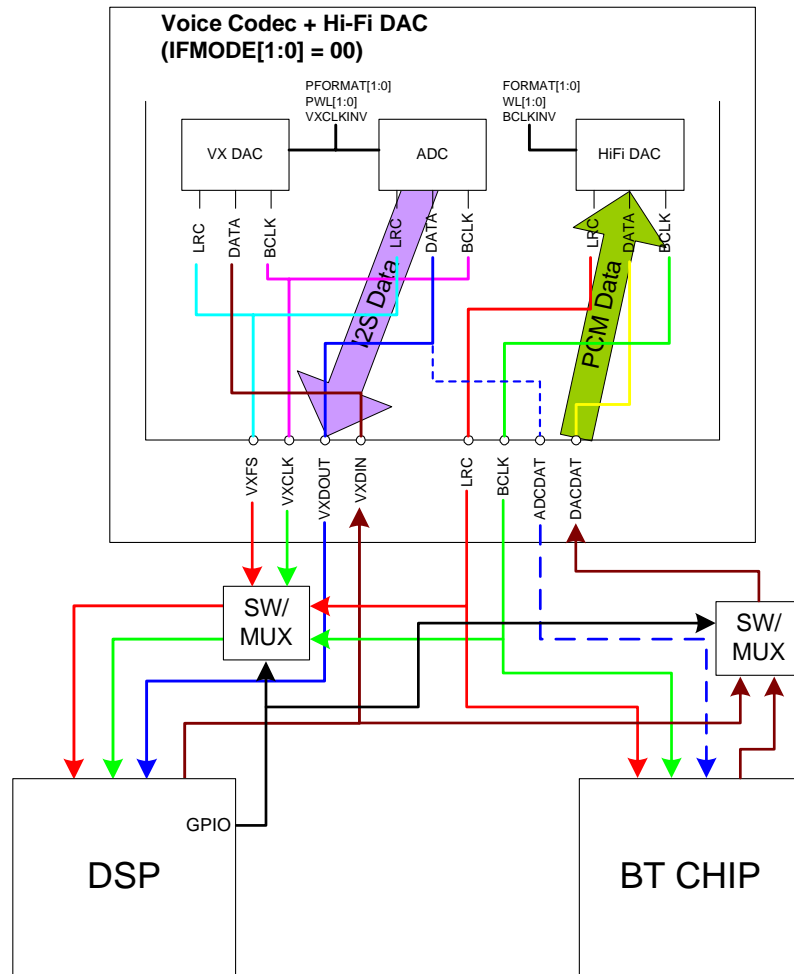
PCM data input to HiFi Interface – I²S data output from Voice Interface

Figure 9 IFMODE[1:0] = 00 Possible Solution 2

Figure 9 shows a possible solution where the HiFi DAC is used for the PCM data input from the BT chip. This allows the PCM data to use a dedicated interface and the I²S data to have its own interface. This has the obvious advantage of allowing each interface to have individual frame sync signals that can be used at different sample rates and high-low pulse widths as required. An example of the interface clocking is shown in Figure 10. It should be noted that the ADC data on VXDOOUT is positioned in the right channel (VXFS high) due to the signal routing path passing through the right ADC only.

The additional sw/mux blocks are required to allow audio playback to be routed through the stereo HiFi DAC from the DSP.

In this mode, the WM8753 can be the Master or Slave.

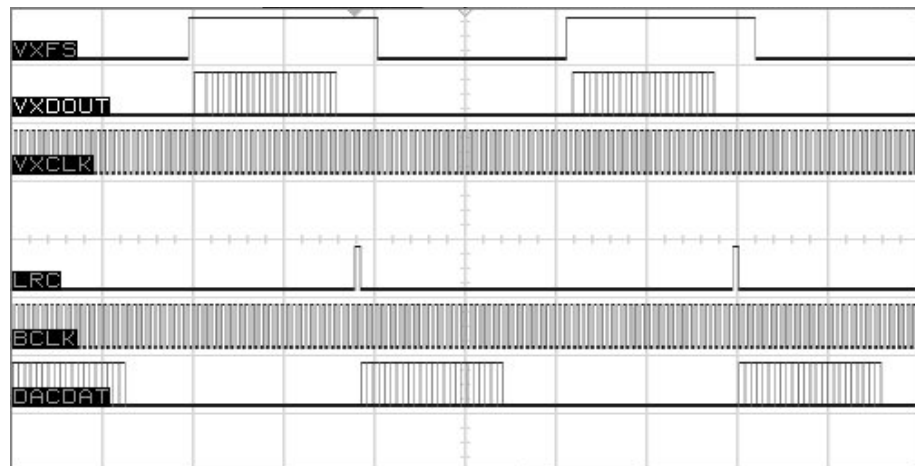


Figure 10 Synchronized I²S Output Data Format

SOLUTION COSIDERATIONS

There are a number of considerations that must be made for either of the suggested solutions within this document. These are summarised in Table 5 for reference.

	SUMMARY	CONSIDERATION
Solution 1	Only one frame sync is available for the PCM to I ² S conversion.	<ol style="list-style-type: none"> 1. <i>Are multiple sample rates required?</i> If so it is not possible to use this solution. 2. <i>Does the BT Chip only require a rising edge on frame sync or does the falling edge have any significance?</i> If the falling edge is a requirement then it is not possible to use this solution unless the DSP can deal with a PCM type frame sync in which case this can be the common format.
	Are all additional signal paths catered for?	There may be many other routing paths required in addition to the PCM to I ² S conversion. The system designer should ensure that all routing is possible around the conversion path.
	A common data clock is used for synchronization purposes.	<i>Can both the BT Chip and the DSP deal with the same data clock rate?</i> This should not be an issue but needs to be confirmed for the relevant IC's used.
	An external switch or multiplexer is required.	The component chosen for this signal selection must be able to deal with switching as fast as the data clock will run.
	The WM8753 must be the Master device.	<i>Can both DSP and BT Chip work as slaves?</i> If not it is not possible to use this solution.

Solution 2	To allow stereo playback through the HiFi DAC, external switches or multiplexers are required.	The components chosen for this signal selection must be able to deal with switching as fast as the data clock will run.
	Are all additional signal paths catered for?	There may be many other routing paths required in addition to the PCM to I ² S conversion. The system designer should ensure that all routing is possible around the conversion path.

Table 5 Solution Comparison

WM8753 SOFTWARE CONSIDERATIONS

The PCM mono mode described in the WM8753 datasheet (Audio Data Formats section) is not a setup option for the HiFi DAC. The HiFi DAC must be set up to work in DSP mode by setting the FORMAT and WL bits found in register R4 (0x04h). Setting the FORMAT[1:0] = 11 sets DSP mode active, the word length may be set between 16 and 32 bits long using the WL[1:0] bits. The word length is system specific.

The ADC should be set to output data in I²S, Left Justified, Right Justified or DSP mode using the PFORMAT[1:0] and PWL[1:0] bits found in register R3 (0x03h).

Please refer to the latest revision of the WM8753 datasheet for more details on the data format and other settings required to set the required path active.

For the list of register settings required to set the routing paths as shown in Figure 11 and Figure 12, refer to Table 6 and Table 7.

CONCLUSION

PCM to I²S data format conversion is a requirement for many new multi-media phone applications.

The WM8753, although not specifically designed for such functionality, does offer the ability to achieve the conversion.

Solution 1 has the advantage of allowing easier internal routing for additional paths with minimal external cost. It does have the limitation that a single frame sync is available relying heavily on a common sample rate being used between the BT Chip and the DSP. It also requires the BT Chip or the DSP to be flexible with the frame syncs that they can accept allowing a common signal to be applied to both. They both must work as slaves with the WM8753 as master to ensure synchronisation.

Solution 2 offers the advantage of two completely independent interfaces that can be run with different data formats at different sample rates. The WM8753 can be master or slave. This solution relies a lot less on the capability of the DSP and BT Chip. The downside is that the cost of external components is higher than solution 1 and the external routing design is slightly more complex.

The solutions offered within this document each have their advantages over the other. The decision over which one is better is system specific and needs to be decided by the system designer based on routing requirements and capability of the DSP and BT Chip used.

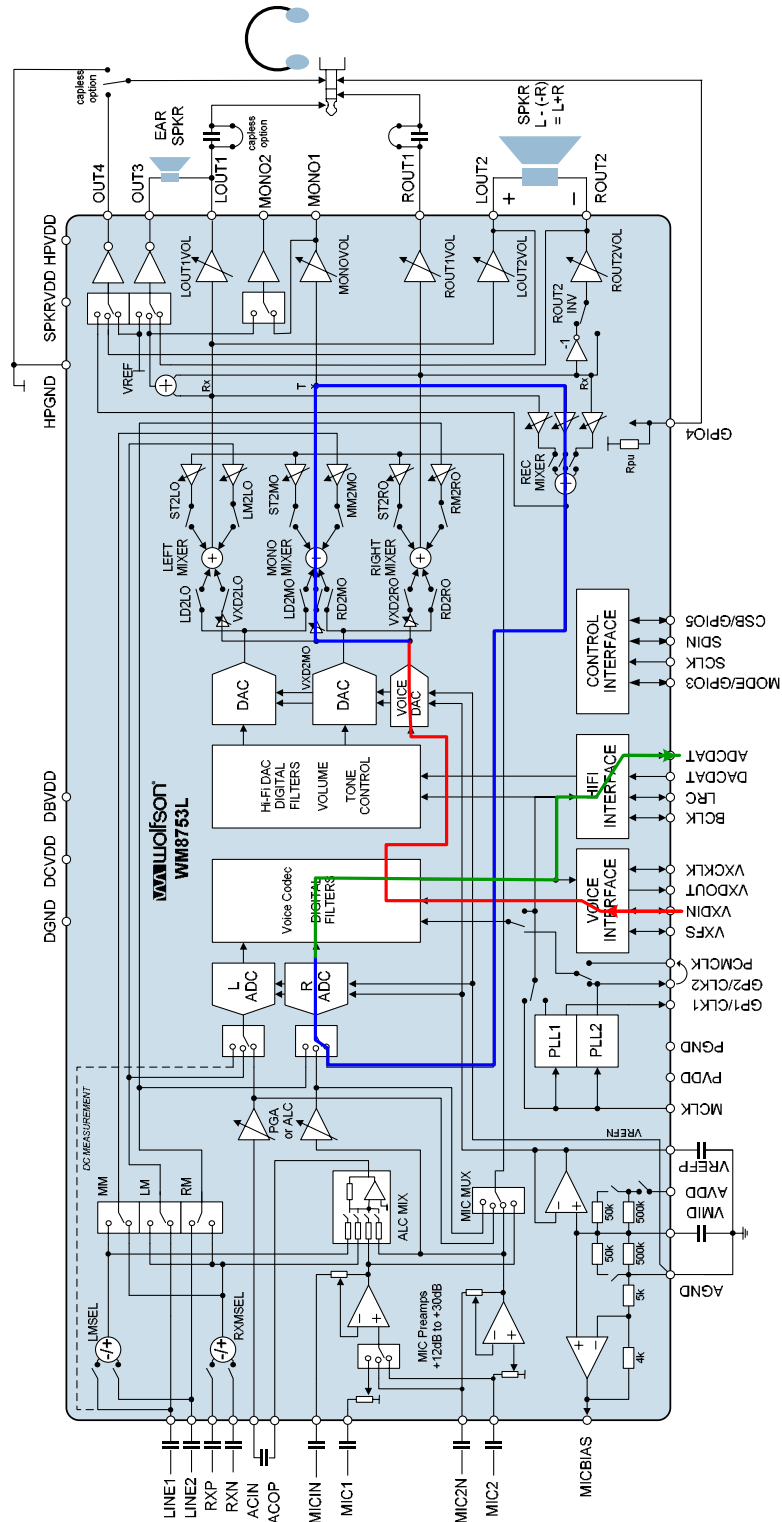


Figure 11 WM8753 Internal Routing Path for Solution 1

REGISTER	VALUE	REGISTER BITS
R3 (03h)	0x14a	ADCDOP=1 [ADC data output to ADCDAT and VXDOUT] PMS=1 [Voice Interface is Master]
R4 (04h)	0x04a	MS=1 [HiFi Interface is Master]
R5 (05h)	0x023	ADCTRI=0 [ADCDAT output is set to standard operation]
R7 (07h)	0x097	PBMODE=010 [VXCLK is equal to MCLK/4] BMODE=010 [BCLK is equal to MCLK/4]
R20 (14h)	0x0d0	VMIDSEL=01 [Power up with 50kΩ] VREF=1 [Power up] VDAC=1 [Power up]
R21 (15h)	0x004	ADCR=1 [Power up]
R23 (17h)	0x00c	RECMIX=1 [Power up] MONOMIX=1 [Power up]
R33 (21h)	0x00a	MSEL=1 [Mono mixer output switched into REC mixer input] MRECVOL=010 [REC mixer volume set to 0dB]
R39 (27h)	0x05b	VXD2MO=1 [Voice DAC output switched into Mono mixer] VXD2MOVOL=011 [VXD2MO volume set to 0dB]
R46 (2eh)	0x008	RADCSEL=10 [REC mixer output selected as RADC input]
Notes:		
<ol style="list-style-type: none"> 1. The register bit descriptions only list changes from default. 2. All other registers and register bits are left in their default state. 		

Table 6 Register Settings Required for the Solution 1 Internal Routing Path

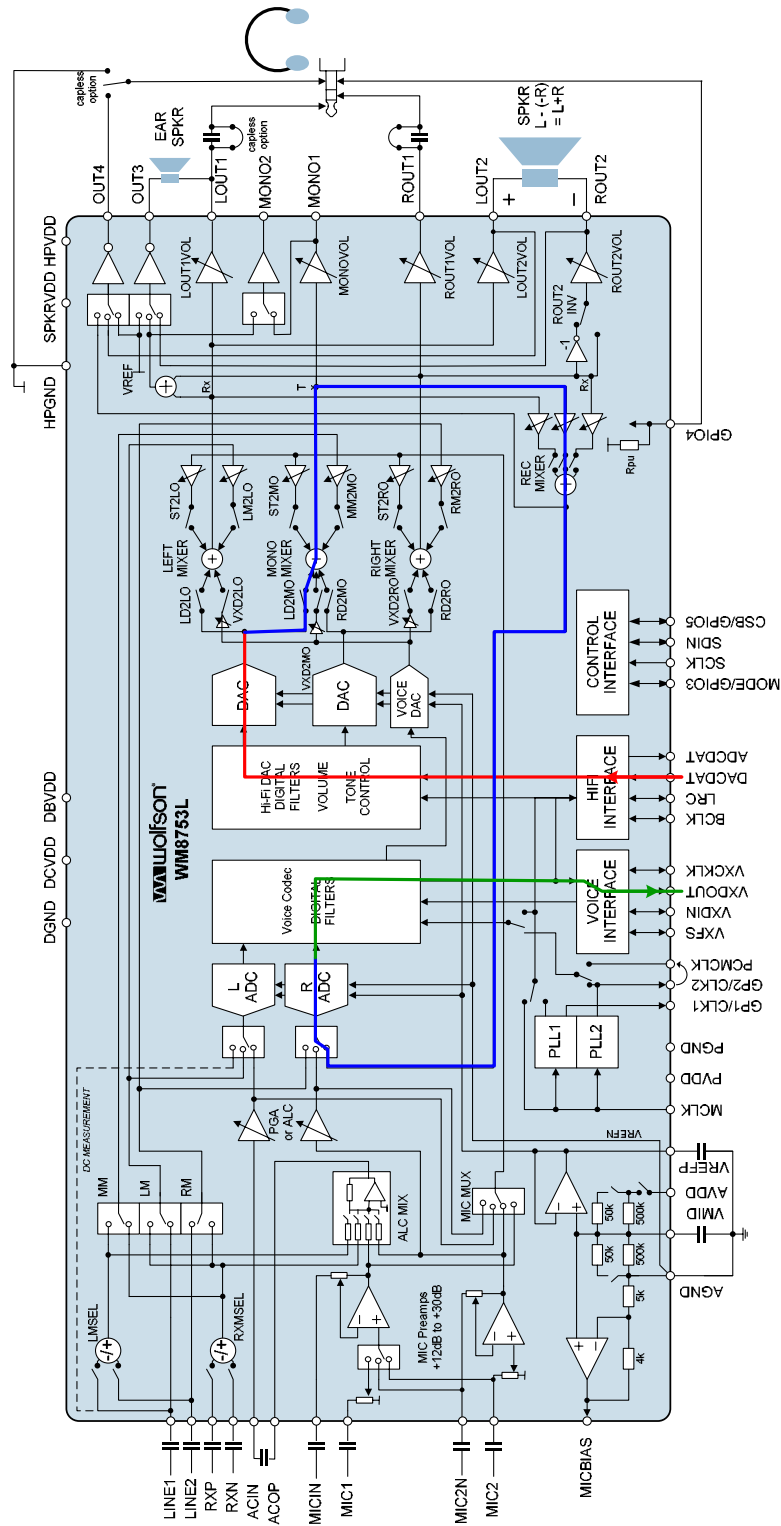


Figure 12 WM8753 Internal Routing Path for Solution 2

REGISTER	VALUE	REGISTER BITS
R1 (01h)	0x000	DACMU=0 [DAC mute off]
R3 (03h)	0x14a	ADCROP=1 [ADC data output to ADCDAT and VXDOUT] PMS=1 [Voice Interface is Master]
R4 (04h)	0x04b	MS=1 [HiFi Interface is Master] FORMAT=11 [DSP mode selected]
R5 (05h)	0x013	VXDTRI=0 [VXDOUT output is set to standard operation]
R7 (07h)	0x097	PBMODE=010 [VXCLK is equal to MCLK/4] BMODE=010 [BCLK is equal to MCLK/4]
R20 (14h)	0x0c8	VMIDSEL=01 [Power up with 50kΩ] VREF=1 [Power up] DACL=1 [Power up]
R21 (15h)	0x004	ADCR=1 [Power up]
R23 (17h)	0x00c	RECMIX=1 [Power up] MONOMIX=1 [Power up]
R33 (21h)	0x008	MSEL=1 [Mono mixer output switched into REC mixer input] MRECVOL=000 [REC mixer volume set to +6dB]
R38 (26h)	0x150	LD2MO=1 [Left DAC switched into Mono mixer]
R46 (2eh)	0x008	RADCSSEL=10 [REC mixer output selected as RADCS input]
Notes:		
<ol style="list-style-type: none"> 1. The register bit descriptions only list changes from default. 2. All other registers and register bits are left in their default state. 		

Table 7 Register Settings Required for the Solution 2 Internal Routing Path

APPLICATION SUPPORT

If you require more information or require technical support please contact Wolfson Microelectronics Applications group through the following channels:

Email: apps@wolfsonmicro.com
Telephone Apps: (+44) 131 272 7070
Fax: (+44) 131 272 7001
Mail: Applications at the address on the last page.

or contact your local Wolfson representative.

Additional information may be made available from time to time on our web site at <http://www.wolfsonmicro.com>

IMPORTANT NOTICE

Wolfson Microelectronics plc (WM) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current. All products are sold subject to the WM terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

WM warrants performance of its products to the specifications applicable at the time of sale in accordance with WM's standard warranty. Testing and other quality control techniques are utilised to the extent WM deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

In order to minimise risks associated with customer applications, adequate design and operating safeguards must be used by the customer to minimise inherent or procedural hazards. Wolfson products are not authorised for use as critical components in life support devices or systems without the express written approval of an officer of the company. Life support devices or systems are devices or systems that are intended for surgical implant into the body, or support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided, can be reasonably expected to result in a significant injury to the user. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

WM assumes no liability for applications assistance or customer product design. WM does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of WM covering or relating to any combination, machine, or process in which such products or services might be or are used. WM's publication of information regarding any third party's products or services does not constitute WM's approval, license, warranty or endorsement thereof.

Reproduction of information from the WM web site or datasheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations and notices. Representation or reproduction of this information with alteration voids all warranties provided for an associated WM product or service, is an unfair and deceptive business practice, and WM is not responsible nor liable for any such use.

Resale of WM's products or services with statements different from or beyond the parameters stated by WM for that product or service voids all express and any implied warranties for the associated WM product or service, is an unfair and deceptive business practice, and WM is not responsible nor liable for any such use.

ADDRESS:

Wolfson Microelectronics plc
26 Westfield Road
Edinburgh
EH11 2QB
United Kingdom

Tel :: +44 (0)131 272 7000

Fax :: +44 (0)131 272 7001

Email :: apps@wolfsonmicro.com